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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/723,687	11/28/2000	Harish G. Patil	1662-23400JMH (PD99-2862)	7608

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EXAMINER	
LI, AIMEE J	

ART UNIT	PAPER NUMBER
2183	

DATE MAILED: 10/02/2003

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/723,687	PATIL ET AL.	
	Examiner	Art Unit	
	Aimee J Li	2183	

-- Th MAILING DATE of this communication app ars on the cover sheet with the correspond nce address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on 28 November 2000 and 29 June 2002 .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-22 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-22 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) 2 and 5 .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

1. Claims 1-22 have been considered.

Papers Submitted

2. It is hereby acknowledged that the following papers have been received and placed of record in the file: IDS as received on 22 August 2001; Request for Refund as received on 04 February 2002; Formal Drawings as received on 23 April 2002; and IDS as received on 28 June 2002.

Specification

3. The abstract of the disclosure is objected to because the first sentence of the abstract refers to "problems noted above" when there is no text prior to the first sentence in the abstract. Correction is required. See MPEP § 608.01(b).

Drawings

4. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they do not include the following reference sign(s) mentioned in the description: page 8, line 5 "L1 cache 16". A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Claim Objections

5. Claim 9 is objected to because of the following informalities: Please correct line 6 from "instructions in said instruction; and" to --instructions in said instruction *queue*; and--. Appropriate correction is required.

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claims 1-3, 7-11, 15-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Mallick et al., U.S. Patent Number 5,752,014 (herein referred to as Mallick) in view of Intel's Intel® IA-64 Architecture Software Developer's Manual Volume 1: IA-64 Application Architecture (herein referred to as Intel Volume 1).

8. Referring to claim 1, Mallick has taught a computer system, comprising:

   a. A processor which includes a hardware branch predictor (Mallick Abstract; column 1, lines 19-31 and 38-55; column 2, line 62 to column 3, line 9; and Figure 1); and

   b. A program of software instructions executed by said processor, said software instructions including conditional branch instructions (Mallick Abstract; column 1, lines 19-31 and 38-55; column 3, line 53 to column 55, line 24; and Figure 1)

9. Mallick has not taught:

   a. Separate static branch prediction instructions;

   b. Said static branch prediction instructions include static branch prediction bits which correspond to conditional branch instructions.

10. Intel Volume 1 has taught:

   a. Separate static branch prediction instructions (Intel Volume 1 pages 4-29 to 4-31, Branch Prediction Hints);

b. Said static branch prediction instructions include static branch prediction bits which correspond to conditional branch instructions (Intel Volume 1 page 4-30 to 4-31, Branch prediction Instructions).

11. A person of ordinary skill in the art at the time the invention was made would have recognized that the information about branch behavior provided by the branch prediction instruction improves branch prediction. Therefore, it would have been obvious to a person of ordinary skill in the art at the time this invention was made to incorporate the branch prediction instructions of Intel Volume 1 in the device of Mallick to improve branch prediction.

12. Referring to claim 9, Mallick has taught a processor, comprising:

a. Fetch logic that fetches program instructions from a source external to said processor (Mallick Abstract; column 3, line 53 to column 4, line 24; column 5, lines 1-12; and Figure 1);

b. A dynamic branch predictor coupled to said fetch logic, said dynamic branch predictor supplies predictions regarding conditional branch instructions to said fetch logic (Mallick Abstract; column 1, lines 19-31 and 38-55; column 2, line 62 to column 3, line 9; and Figure 1);

c. An instruction queue coupled to said dynamic predictor, said fetch logic storing fetched instructions in said instruction queue (Mallick Abstract; column 3, line 53 to column 4, line 24); and

d. An execution unit coupled to said instruction queue and executing instructions provided from said instruction queue (Mallick Abstract column 1, lines 19-31 and 38-55; column 2, line 69 to column 3, line 2; and column 5, lines 25-42);

13. Mallick has not taught said fetch logic examines fetched instructions for a predetermined register identifier that identifies that instruction as a static branch prediction instruction that provides static branch prediction information about other fetched instructions. Intel Volume 1 has taught said fetch logic examines fetched instructions for a predetermined register identifier that identifies that instruction as a static branch prediction instruction that provides static branch prediction information about other fetched instructions (Intel Volume 1 page 4-29). In regards to Intel Volume 1, it must be determined whether a branch prediction instruction exists in order for the processor to chose whether to ignore the instruction or not and it does not matter whether the processor determines this in the fetch or not, because it functions the same. A person of ordinary skill in the art at the time the invention was made would have recognized that the information about branch behavior provided by the branch prediction instruction improves branch prediction. Therefore, it would have been obvious to a person of ordinary skill in the art at the time this invention was made to incorporate the branch prediction instructions of Intel Volume 1 in the device of Mallick to improve branch prediction.

14. Referring to claims 2-3, 7, 10-11, 15, 17, and 19-20 Mallick has not taught:

a. Wherein said program includes one static branch prediction instruction for each group of n other instructions (Applicant's claims 2, 10, and 19);

b. Wherein n is 7 (Applicant's claims 3, 11, and 20);

c. Wherein said static branch prediction bits include static branch prediction information that includes encoded information directing the processor to ignore the predictions supplied by the hardware branch predictor (Applicant's claims 7 and 15);

d. Wherein said predetermined identifier comprises a register identifier (Applicant's claim 17).

15. Intel Volume 1 has taught:

a. Wherein said program includes one static branch prediction instruction for each group of n other instructions (Applicant's claims 2, 10, and 19) (Intel Volume 1 page 4-30 to 4-31, Branch prediction Instructions). In regards to Intel Volume 1, the purpose of a static branch prediction instruction is to provide information about future branches in a group of instructions, so the static branch prediction instruction must be part of the same group of instructions where the branch exists.

b. Wherein n is 7 (Applicant's claims 3, 11, and 20) (Intel Volume 1 page 4-30 to 4-31, Branch Prediction Instructions). In regards to Intel Volume 1, the purpose of a static branch prediction instruction is to provide information about future branches in a group of instructions, so the static branch prediction instruction must be part of the same group of instructions where the branch exists. The size of the group is an arbitrary number.

c. Wherein said static branch prediction bits include static branch prediction information that includes encoded information directing the processor to ignore the predictions supplied by the hardware branch predictor (Applicant's claims 7 and 15) (Intel Volume 1 page 4-30 to page 4-31, Branch Prediction Instructions).

d. Wherein said predetermined identifier comprises a register identifier (Applicant's claim 17) (Intel Volume 1 page 4-29).

16. A person of ordinary skill in the art at the time the invention was made would have recognized that the information about branch behavior provided by the branch prediction instruction improves branch prediction. Therefore, it would have been obvious to a person of ordinary skill in the art at the time this invention was made to incorporate the branch prediction instructions of Intel Volume 1 in the device of Mallick to improve branch prediction.

17. Referring to claims 8 and 16, Mallick has taught wherein said hardware branch predictor includes a log in which the results of all executed conditional branch instructions are stored (Mallick column 2, lines 10-15; column 6, lines 63-67; column 7, lines 36-54; Figure 2, element 68; and Figure 3).

18. Referring to claim 18, Mallick has taught a method of predicting the outcome of conditional branch instructions, comprising:

a. Including a static branch predictor software instruction in a program, said branch prediction software instruction including branch prediction information pertaining to other instructions in the program (Intel Volume 1 pages 4-30 to 4-31, Branch Prediction Instructions);

b. Fetching said branch prediction software instructions (Mallick Abstract; column 3, line 53 to column 3, line 24; column 5, lines 1-12; and Figure 1);

c. Decoding said branch prediction software instructions to determine if said decoded instruction is a branch prediction software instruction (Mallick Abstract; column 1, lines 19-31 and 38-55; column 2, line 62 to column 3, line 9; column 3, line 53 to column 4, line 24; column 5, lines 13-24; and Figure 1).

19. Mallick has not taught if said decoded instruction is a branch prediction software instruction, then using said branch prediction information for branch prediction. Intel Volume 1 has taught if said decoded instruction is a branch prediction software instruction, then using said branch prediction information for branch prediction (Intel Volume 1 pages 4-30 to 4-31, Branch Prediction Instructions). A person of ordinary skill in the art at the time the invention was made would have recognized that the information about branch behavior provided by the branch prediction instruction improves branch prediction. Therefore, it would have been obvious to a person of ordinary skill in the art at the time this invention was made to incorporate the branch prediction instructions of Intel Volume 1 in the device of Mallick to improve branch prediction.

20. Claims 4-6, 12-14, and 21-22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Mallick in view of Intel Volume 1, as applied to claim 2 above, and further in view of Intel's Intel® Itanium® Architecture Software Developer's Manual Volume 3: Instruction Set Reference (herein referred to as Intel Volume 3).

21. Referring to claims 4, 12, and 21, Mallick has not taught wherein said static branch prediction bits included in a static branch prediction instruction include pairs of prediction bits, each pair providing prediction information for a separate instruction in said group of n other instructions (Intel Volume 3 page 3:317 to 3:319, Branch Predict/Nop/Hint). Intel Volume 3 has taught wherein said static branch prediction bits included in a static branch prediction instruction include pairs of prediction bits, each pair providing prediction information for a separate instruction in said group of n other instructions (Applicant's claim 4) (Intel Volume 3 page 3:317 to 3:319, Branch Predict/Nop/Hint). A person of ordinary skill in the art at the time the invention was made would have recognized that the information about branch behavior provided

by the branch prediction instruction improves branch prediction. Therefore, it would have been obvious to a person of ordinary skill in the art at the time this invention was made to incorporate the branch prediction instructions of Intel Volume 3 in the device of Mallick to improve branch prediction.

22. Referring to claims 5-6, 13-14, and 22, Mallick has not taught:

a. Wherein said prediction information includes a member selected from the group consisting of: do not use static prediction, predict taken, and predict not taken (Applicant's claims 5, 13, and 22);

b. Wherein each pair of prediction bits corresponds to another instruction and each pair of prediction bits is encoded as: 00 and 01 mean do not use static prediction, 10 means predict taken and 11 means predict not taken (Applicant's claims 6 and 14).

23. Intel Volume 1 has taught:

a. Wherein said prediction information includes a member selected from the group consisting of: do not use static prediction, predict taken, and predict not taken (Applicant's claim 5, 13, and 22) (Intel Volume 1 page 4-30 to page 4-31, Branch Prediction Instructions).

b. Wherein each pair of prediction bits corresponds to another instruction and each pair of prediction bits is encoded as: 00 and 01 mean do not use static prediction, 10 means predict taken and 11 means predict not taken (Applicant's claims 6 and 14) (Intel Volume 1 page 4-30 to page 4-31, Branch Prediction Instructions). In regards to Intel Volume 1, the exact bit representations do not matter, because the

functionality is the same. The exact bit representations are more of a design choice than inventive matter.

24. A person of ordinary skill in the art at the time the invention was made would have recognized that the information about branch behavior provided by the branch prediction instruction improves branch prediction. Therefore, it would have been obvious to a person of ordinary skill in the art at the time this invention was made to incorporate the branch prediction instructions of Intel Volume 1 in the device of Mallick to improve branch prediction.

Conclusion

25. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure as follows. Applicant is reminded that in amending in response to a rejection of claims, the patentable novelty must be clearly shown in view of the state of the art disclosed by the references cited and the objections made. Applicant must also show how the amendments avoid such references and objections. See 37 CFR § 1.111(c).

a. Rahman et al., U.S. Patent Number 5,805,878, has taught a branch prediction device with both dynamic and static methods.

b. Lempel, U.S. Patent Number 5,978,909, has taught a branch prediction device with both dynamic and static methods.

c. Henry et al., U.S. Patent Number 6,247,122, has taught a branch prediction device with both dynamic and static methods.

d. Henry et al., U.S. Patent Number 6,499,101, has taught a branch prediction device with both dynamic and static methods.

e. Henry et al., U.S. Patent Number 6,550,004, has taught a branch prediction device with both dynamic and static methods.

f. Harish Patil and Hoel Emer, "Combining Static and Dynamic Branch Prediction to Reduce Destructive Aliasing", has taught a branch prediction device with both dynamic and static methods.

26. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Aimee J Li whose telephone number is (703) 305-7596. The examiner can normally be reached on M-T 7:30am-5:00pm.

27. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (703) 305-9712. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 746-7239 for regular communications and (703) 746-7238 for After Final communications.

28. Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 305-3900.

Aimee J. Li
Examiner
Art Unit 2183

September 29, 2003

EDDIE CHAN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100